CLAIMS

1. A method for making error corrections on digital information coded as symbol sequences, for example digital information stored in electronic memory systems or transmitted from and to these systems providing the transmission of sequences incorporating a portion of error corrector code allowing the sequence which is more probably the original transmitted through the calculation of an error syndrome using a parity matrix to be restored when received, characterized in that the error code incorporated in the original sequence belongs to a non Boolean group.

2. A method according to claim 1, characterized in that said error code is a linear code.

3. A method according to claim 1, characterized in that said error code recognizes an error of the $0 \rightarrow 1$ type from an error of the $1 \rightarrow 0$ type.

4. A method according to claim 1, characterized in that said parity matrix comprises an identity matrix having a determinant different from 0, i.e. that a number belonging to the matrix is not a linear combination of other numbers belonging to the same matrix and if in an additive group mod p with p different from 2 it is composed of the numbers p-1, p-2, ..., $p-2^{n-k}$.

5. A method according to claim 1, characterized in that said error code belongs to an Abelian group.

6. A method according to claim 1, characterized in that said error code is a code in the systematic form.

7. A method for generating an error correcting code, comprising:

developing data bits to be encoded;

generating a non-binary group of values; and

generating the error correcting code from the non-binary group of values and the data bits.

8. The method of claim 7 wherein the non-binary group of values is generated by performing non-binary addition.

9. The method of claim 8 wherein the non-binary addition is performed on binary values.

10. The method of claim 7 wherein the error correcting code comprises a linear code.

11. The method of claim 7 wherein the error correcting code differentiates between an error wherein a binary value changes from a binary 0 to a binary 1 and an error wherein a binary value changes from a binary 1 to a binary 0.

12. The method of claim 7 wherein a parity matrix comprises an identity matrix having a determinant different from 0 that is utilized in generating the error correcting code.

13. The method of claim 12 wherein the columns of the parity matrix have additive group values of mod p with p different from 2 and being composed of the numbers p-1, p-2, ..., $p-2^{n-k}$.

14. An error detection and correction circuit, comprising:

a plurality of non-binary adder circuits, each non-binary adder circuit operable to generate a non-binary group of values adapted to be applied to a data word being encoded to develop an error detecting and correcting code corresponding to the data word.

15. The error detection and correction circuit of claim 14 wherein each non-binary adder circuit operates on binary values.

16. The error detection and correction circuit of claim 14 wherein the error detecting and correcting code comprises a linear code.

17. The error detection and correction circuit of claim 14 wherein the generated error correcting code differentiates between an error wherein a binary value changes from a binary 0 to a binary 1 and an error wherein a binary value changes from a binary 1 to a binary 0.

18. The error detection and correction circuit of claim 14 wherein the adder circuits form a parity matrix comprising an identity matrix having a determinant different from 0, with the parity matrix being utilized in generating the error correcting code.

19. The error detection and correction circuit of claim 18 the columns of the parity matrix have additive group values of mod p with p different from 2 and being composed of the numbers p-1, p-2, ..., $p-2^{n-k}$.

20. An electronic system, comprising:

an error detection and correction circuit, including,

a plurality of non-binary adder circuits, each non-binary adder circuit operable to generate a non-binary group of values adapted to be applied to a data word being encoded to develop an error detecting and correcting code corresponding to the data word.

21. The electronic system of claim 20 wherein the system comprises a memory system of a computer system.